

FEATURES

Single-supply operation: 4.5 V to 16.5 V
Upper/lower buffers swing to V_S/GND
Continuous output current: 35 mA
V_{COM} peak output current: 250 mA
Offset voltage: 15 mV
Slew rate: 6 V/μs
Unity gain stable with large capacitive loads
Supply current: 750 μA per amplifier

APPLICATIONS

TFT LCD monitor panels
TFT LCD notebook panels
Communications equipment
Portable instrumentation
Electronic games
ADC/DAC buffer

GENERAL DESCRIPTION

The ADD8706 is a single-supply, 5-channel buffer with a separate V_{COM} amplifier that has been optimized for today's low cost TFT LCD notebook and monitor panels. The top and bottom channels swing to the top/bottom rails, respectively, and can be used as end-point gamma references. The middle channels are ideal for midpoint gamma references. The V_{COM} amplifier provides very high continuous and peak currents. All channels have excellent transient response as well as high slew rate and capacitive load drive capability. The ADD8706 is specified over the -40°C to +85°C temperature range. The ADD8706 is available in a 16-lead TSSOP package.

Table 1. Input Output Characteristics

Channel	V _{IH}	V _{IL}	I _O (mA)	I _{SC} (mA)
A	V _S	GND + 1.7 V	15	150
B	V _S - 1.7 V	GND	15	150
C	V _S - 1.7 V	GND	15	150
D	V _S - 1.7 V	GND	15	150
E	V _S - 1.7 V	GND	15	150
F	V _S - 1.7 V	GND	35	250

PIN CONFIGURATION

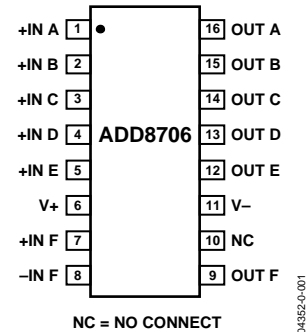


Figure 1. 16-Lead TSSOP

Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

Electrical Characteristics	3	Theory.....	9
Absolute Maximum Ratings.....	5	Input/Output Characteristics	9
ESD Caution.....	5	Important Note.....	9
Typical Performance Characteristics	6	Outline Dimensions	11
Application Information.....	9	Ordering Guide	11

REVISION HISTORY

Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS

Table 2. $V_S = 16\text{ V}$, $V_{CM} = V_S/2$, $T_A @ 25\text{ }^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SUPPLY CHARACTERISTICS						
Supply Voltage	V_S		4.5		16	V
Power Supply Rejection Ratio	PSRR	$V_S = 4\text{ V to }17\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	70	90		dB
Total Supply Current	I_{SY}	$V_O = V_S/2$, No Load $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		4.5	5.4 6	mA mA
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			2	15	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		10		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		400	1100 1500	nA nA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		10	100	nA
Amplifier F		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			250	nA
Common-Mode Rejection Ratio	CMRR	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$				
Amplifier F		$V_{CM} = 0$ to $(V_S - 1.7\text{ V})$	54	95		dB
Input Impedance	Z_{IN}			400		k Ω
Input Capacitance	C_{IN}			1		pF
OUTPUT CHARACTERISTICS						
Output Voltage High (A)	V_{OH}	$V_{IN} = 16\text{ V}$, $I_L = 100\text{ }\mu\text{A}$		15.99		V
Optimized for High Swing		$V_{IN} = 16\text{ V}$, $I_L = 5\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	15.75 15.65	15.85		V V
Output Voltage High (B to D)	V_{OH}	$V_{IN} = 14\text{ V}$, $I_L = 100\text{ }\mu\text{A}$		14		V
Optimized for Midrange		$V_{IN} = 14\text{ V}$, $I_L = 5\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	13.90 13.85	13.985		V V
Output Voltage High (E)	V_{OH}	$V_{IN} = 14\text{ V}$, $I_L = 100\text{ }\mu\text{A}$		14		V
Optimized for Low Swing		$V_{IN} = 14\text{ V}$, $I_L = 5\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	13.9 13.85	13.99		V V
Output Voltage High (F)	V_{OH}	$V_{IN} = 16\text{ V}$, $I_L = 100\text{ }\mu\text{A}$		15.995		V
Optimized for V_{COM}		$V_{IN} = 16\text{ V}$, $I_L = 5\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	15.8 15.75	15.9		V V
Output Voltage Low (A)	V_{OL}	$V_{IN} = 1.7\text{ V}$, $I_L = 100\text{ }\mu\text{A}$		1.70		V
Optimized for High Swing		$V_{IN} = 1.7\text{ V}$, $I_L = 5\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		1.71	1.730 1.725	V V
Output Voltage Low (B–D)	V_{OL}	$V_{IN} = 0\text{ V}$, $I_L = 100\text{ }\mu\text{A}$		5		mV
Optimized for Midrange		$V_{IN} = 0\text{ V}$, $I_L = 5\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		200	300 350	mV mV
Output Voltage Low (E)	V_{OL}	$V_{IN} = 0\text{ V}$, $I_L = 100\text{ }\mu\text{A}$		5		mV
Optimized for Low Swing		$V_{IN} = 0\text{ V}$, $I_L = 5\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		80	200 300	mV mV
Output Voltage Low (F)	V_{OL}	$V_{IN} = 0\text{ V}$, $I_L = 100\text{ }\mu\text{A}$		5		mV
Optimized for V_{COM}		$V_{IN} = 0\text{ V}$, $I_L = 5\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		50	150 250	mV mV
Continuous Output Current (A to E)	I_{OUT}	$V_S = 16\text{ V}$		15		mA
Continuous Output Current (F)	I_{OUT}	$V_S = 16\text{ V}$		35		mA
Peak Output Current (A to E)	I_{PK}	$V_S = 16\text{ V}$		50		mA
Peak Output Current (F)	I_{PK}	$V_S = 16\text{ V}$		200		mA

ADD8706

Parameter	Symbol	Condition	Min	Typ	Max	Unit
TRANSFER CHARACTERISTICS						
Amplifier Gain	A_{vo}	$R_L = 2\text{ k}\Omega, V_o = 0.5\text{ to } (V_s - 2\text{ V})$	1	10		V/mV
Buffer Gain	A_{vcl}	$R_L = 2\text{ k}\Omega$	0.995	0.9985	1.005	V/V
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	0.995	0.9980	1.005	V/V
Buffer Gain Linearity	NL	$R_L = 2\text{ k}\Omega, V_o = 0.5\text{ to } (V_s - 0.5\text{ V})$		0.01		%
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega, C_L = 200\text{ pF}$	4	6		V/ μs
Bandwidth	BW	$-3\text{ dB}, R_L = 2\text{ k}\Omega, C_L = 40\text{ pF}$		6		MHz
Phase Margin	ϕ_o	$R_L = 2\text{ k}\Omega, C_L = 40\text{ pF}$		55		Degrees
Channel Separation				75		dB
NOISE PERFORMANCE						
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		26		nV/ $\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		25		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 10\text{ kHz}$		0.8		pA/ $\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Table 3. ADD8706 Stress Ratings*

Parameter	Rating
Supply Voltage (V_s)	18 V
Input Voltage	-0.5 V to $V_s + 0.5$ V
Differential Input Voltage	V_s
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature Range	300°C
ESD Tolerance (HBM)	±1500 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table 4. Package Characteristics

Package Type	θ_{JA} ¹	θ_{JC}	Unit
16-Lead TSSOP (RU)	180	35	°C/W

¹ θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for devices soldered onto a circuit board for surface-mount packages.



TYPICAL PERFORMANCE CHARACTERISTICS

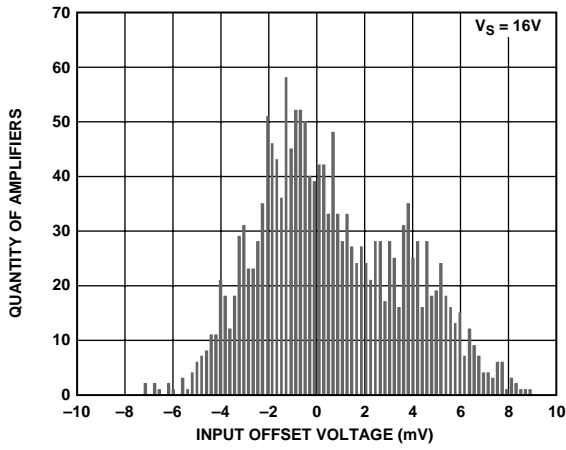


Figure 2. Input Offset Voltage, $V_S = 16\text{ V}$

04352-0-025

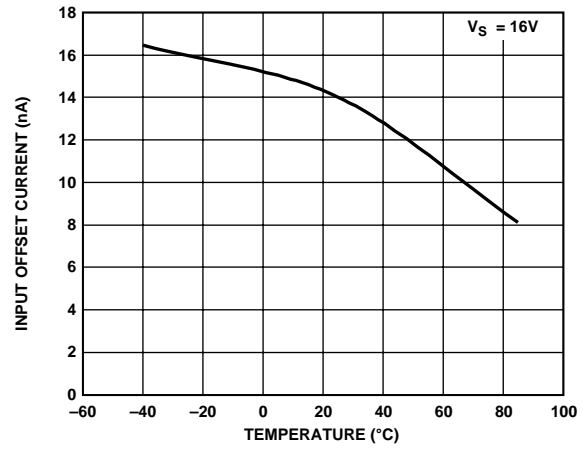


Figure 5. Input Offset Current vs. Temperature

04352-0-028

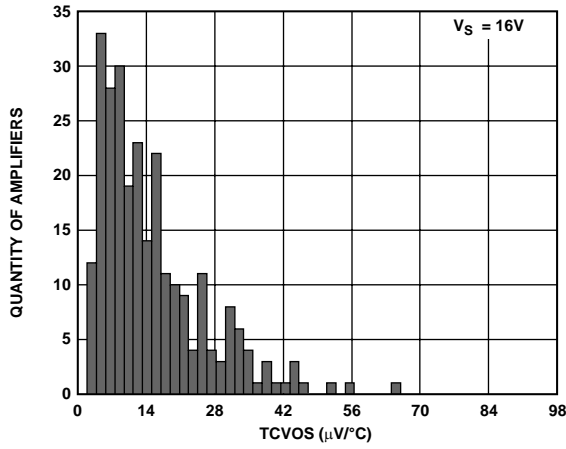


Figure 3. Input Offset Voltage Drift, $V_S = 16\text{ V}$

04352-0-026

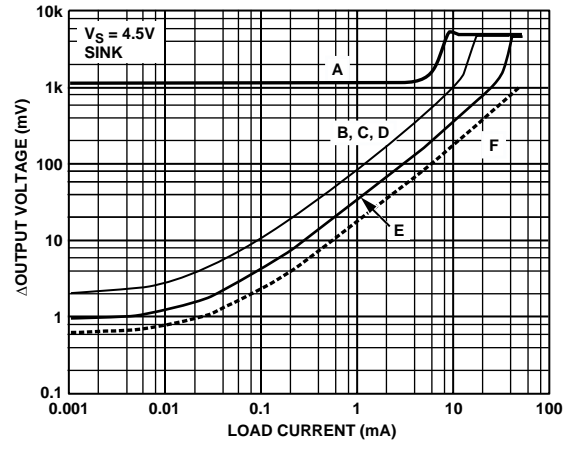


Figure 6. Output Sink Voltage vs. Load Current, All Channels

04352-0-013

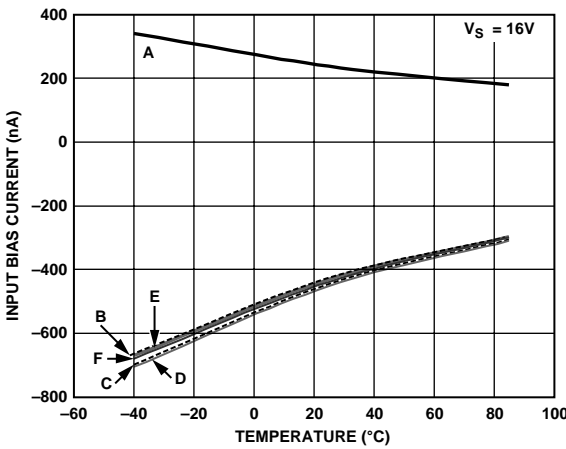


Figure 4. Input Bias Current vs. Temperature

04352-0-027

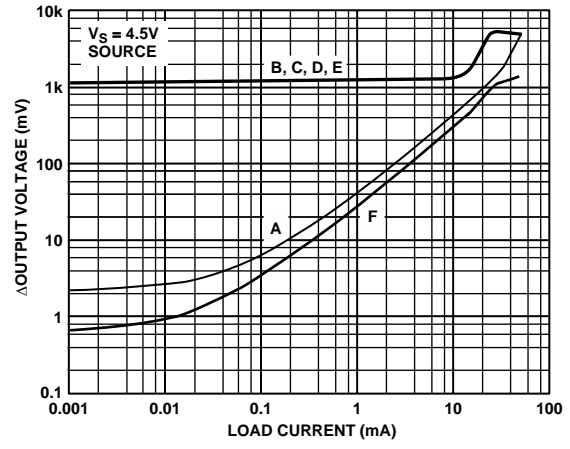


Figure 7. Output Source Voltage vs. Load Current, All Channels

04352-0-015

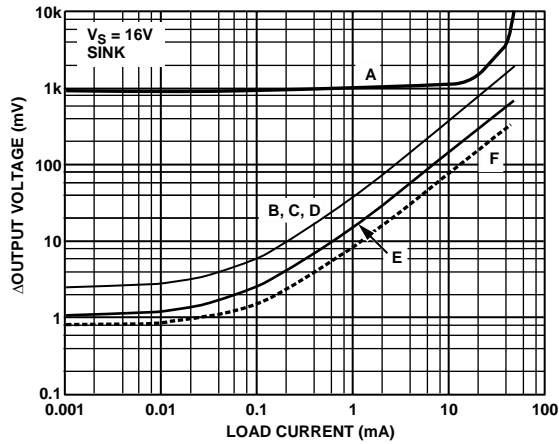


Figure 8. Output Sink Voltage vs. Load Current, All Channels

04352-0-014

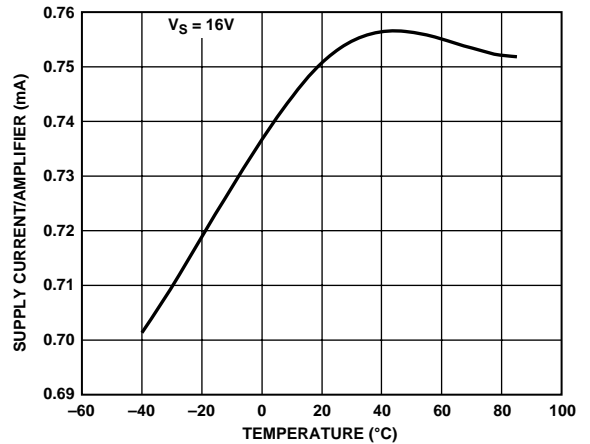


Figure 11. Supply Current vs. Temperature

04352-0-029

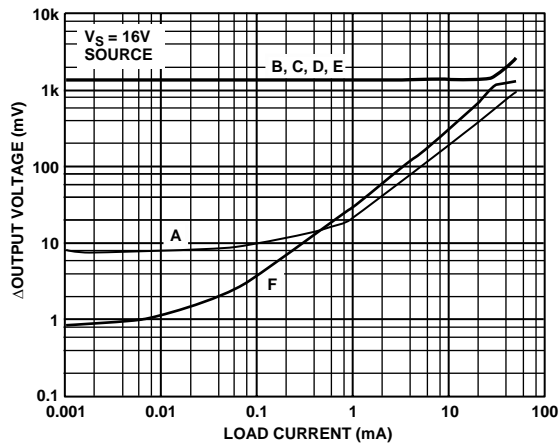


Figure 9. Output Source Voltage vs. Load Current, All Channels

04352-0-016

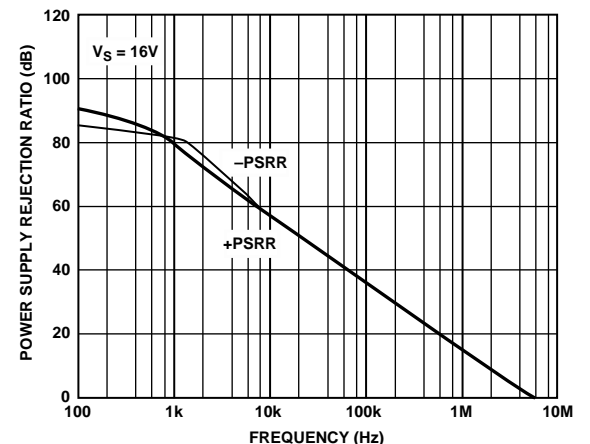


Figure 12. PSRR vs. Frequency

04352-0-018

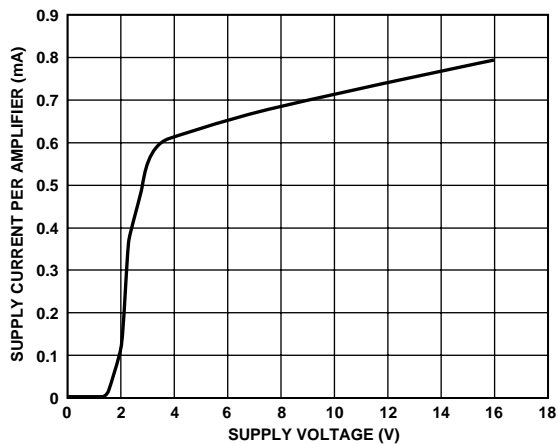


Figure 10. Supply Current vs. Supply Voltage

04352-0-022

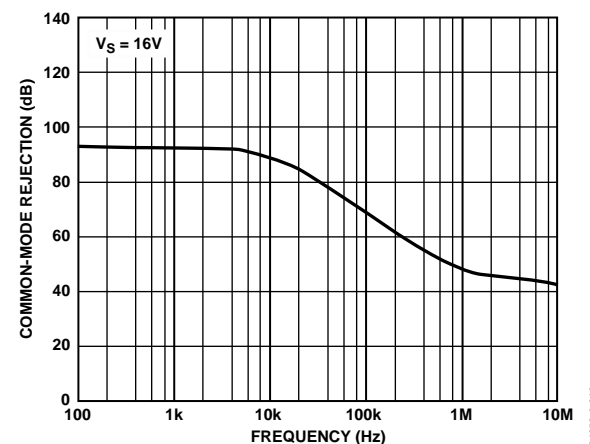


Figure 13. CMRR vs. Frequency

04352-0-010

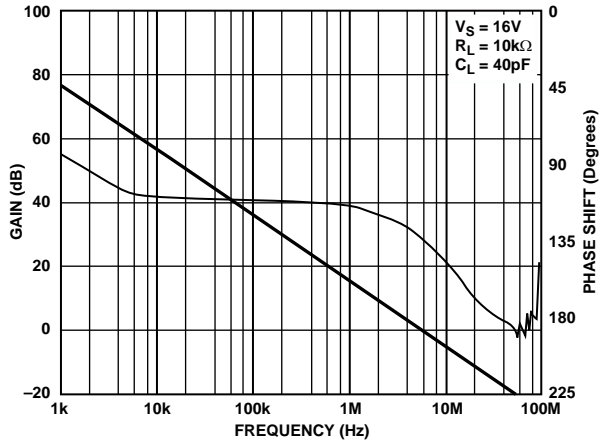


Figure 14. Frequency vs. Gain and Shift

04352-0-012

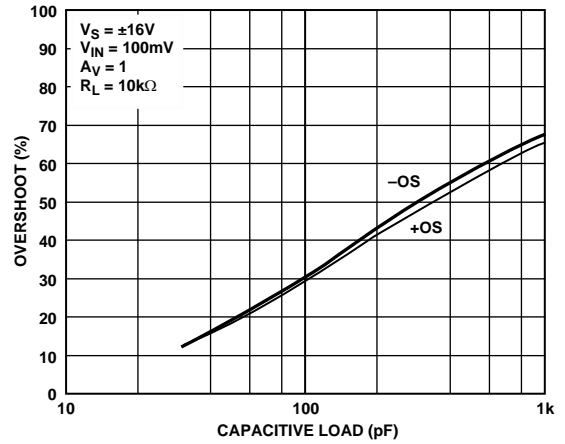


Figure 17. Overshoot vs. Capacitive Load

04352-0-020

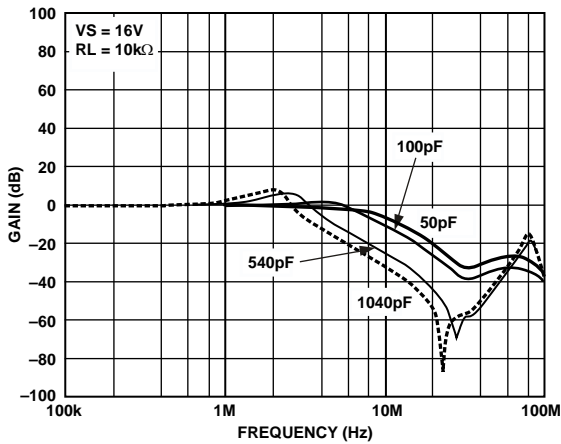


Figure 15. Gain vs. Capacitive Load

04352-0-008

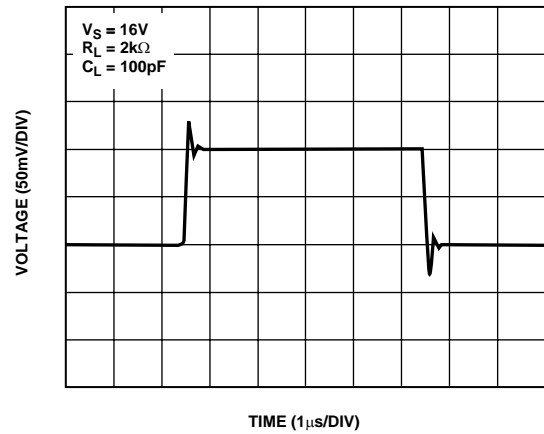


Figure 18. Small-Signal Transient Response

04352-0-021

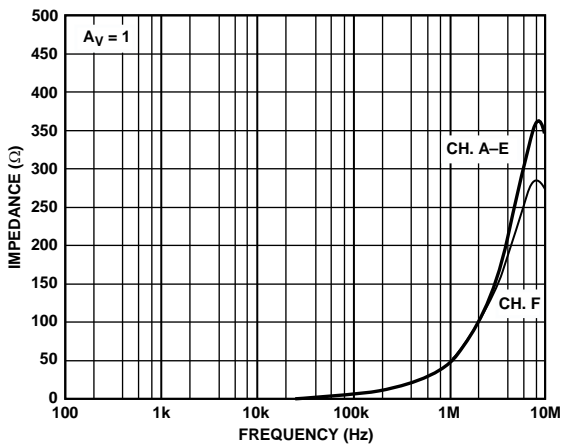


Figure 16. Impedance vs. Frequency

04352-0-005

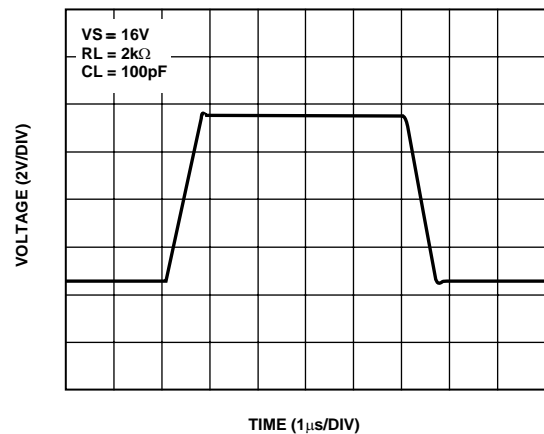


Figure 19. Large Signal Transient Response

04352-0-013

ADD8706

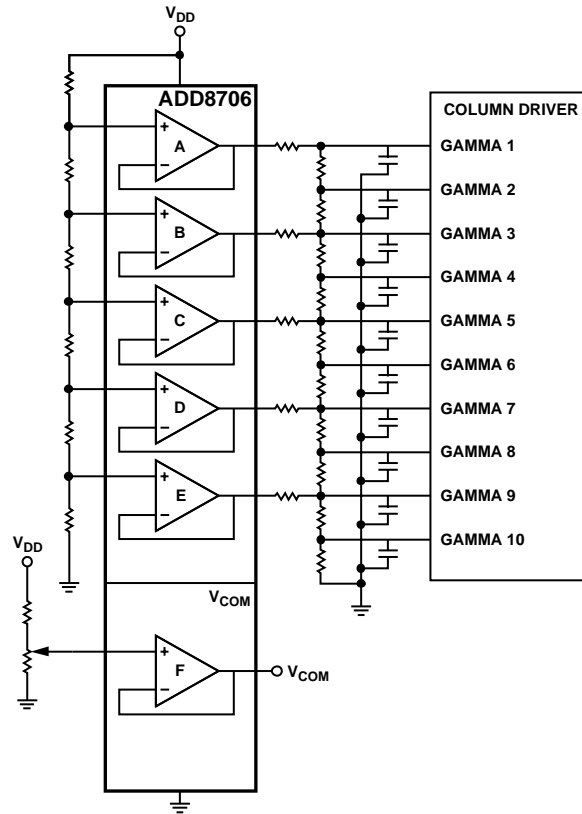
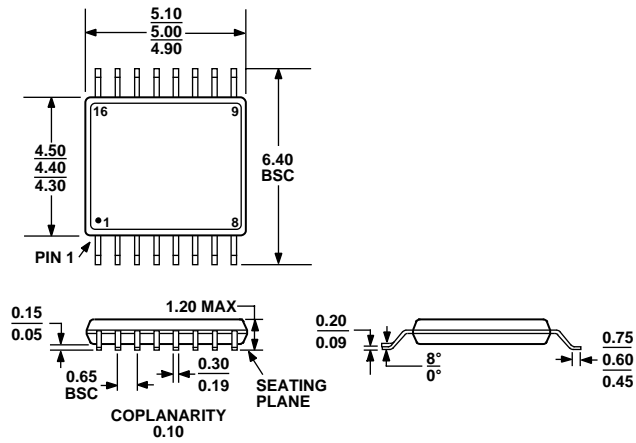


Figure 21. ADD8706 Application Circuit

000004-000

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153AB

Figure 22. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU)
Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADD8706ARUZ	-40°C to +85°C	16-Lead TSSOP	RU-16
ADD8706ARUZ-REEL	-40°C to +85°C	16-Lead TSSOP	RU-16

¹ Z = Pb-free part.

ADD8706

NOTES